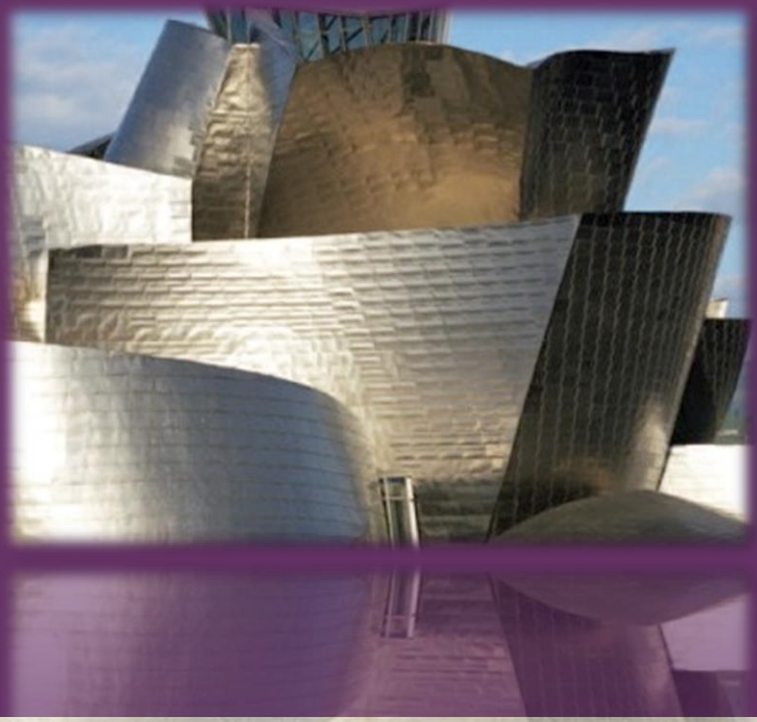


William Stallings Computer Organization and Architecture 10th Edition

Chapter 3 – Part 2

A top-level view of computer function and interconnection

计算机功能和互连的顶层视图

Outline

2. The computer system

2.1 A Top-Level View of Computer Function and Interconnection

2.2 Cache Memory

2.3 Internal Memory Technology

2.4 External Memory

2.5 Input/Output

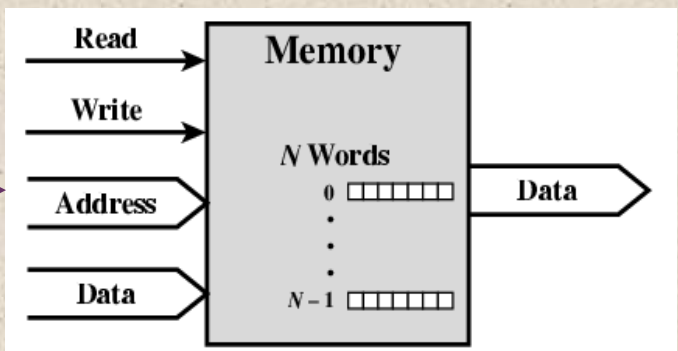
4- Interconnection Structures
互连结构

- A computer consists of modules of three basic types (processor, memory, I/O) that communicate with each other. Thus, there must be paths for connecting the modules.
- The collection of paths connecting the various modules is called the *interconnection structure*. The design of this structure will depend on the exchanges that must be made among modules.
- Different type of connection for different type of unit
  - Memory
  - Input/Output
  - CPU

Computer Modules

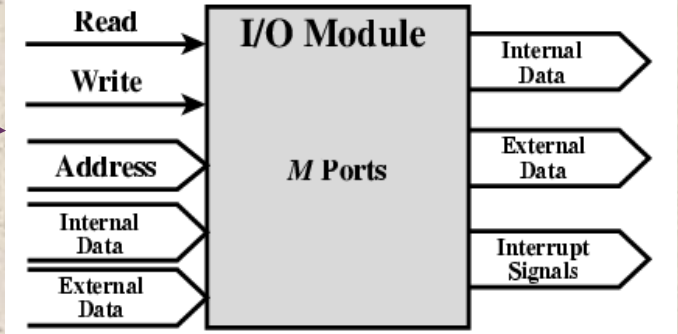
Memory Connection

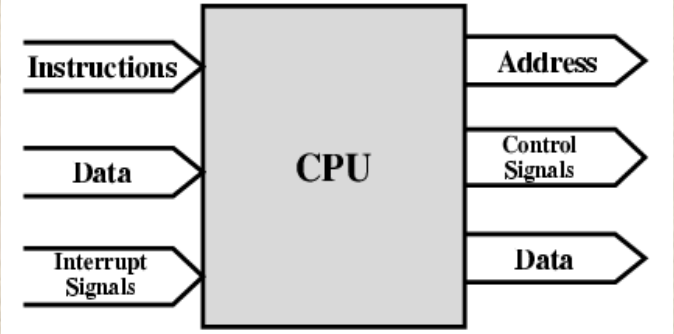
- Receives and sends data
- Receives addresses (of locations)
- Receives control signals
  - Read
  - Write
  - Timing



Input/Output Connection(1)

- Similar to memory from computer's viewpoint
- Output
  - Receive data from computer
  - Send data to peripheral
- Input
  - Receive data from peripheral
  - Send data to computer
- Receive control signals from computer
- Send control signals to peripherals
  - e.g. spin disk
- Receive addresses from computer
  - e.g. port number to identify peripheral
- Send interrupt signals (control)

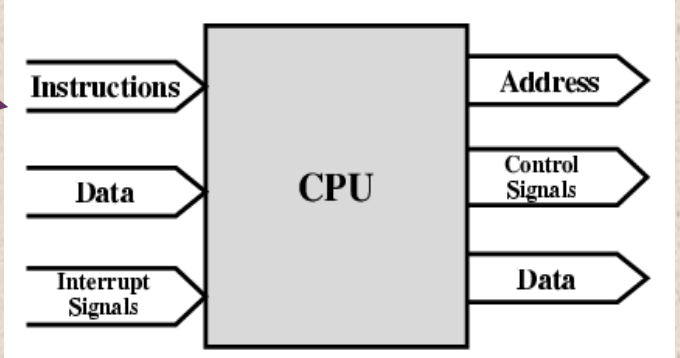




Computer Modules

CPU Connection

- Reads instruction and data
- Writes out data (after processing)
- Sends control signals to other units
- Receives (& acts on) interrupts



- The last list defines the data to be exchanged. The interconnection structure must support the following types of transfers. Next slide

- Over the years, a number of interconnection structures have been tried.
- By far the most common are (1) the bus and various multiple-bus structures, and (2) point-to-point interconnection structures with packetized data transfer.

The interconnection structure must support the following types of transfers:

Memory to processor	Processor to memory	I/O to processor	Processor to I/O	I/O to or from memory
Processor reads an instruction or a unit of data from memory	**Processor writes a unit of data to memory**	**Processor reads data from an I/O device via an I/O module**	**Processor sends data to the I/O device**	**An I/O module is allowed to exchange data directly with memory without going through the processor using direct memory access**

A- Bus Interconnection

A communication pathway connecting two or more devices

- Key characteristic is that it is a shared transmission medium

Signals transfered by any one device are available for reception by all other devices attached to the bus

- If two devices transmit during the same time period their signals will overlap and become garbled

Typically consists of multiple communication lines

- Each line is capable of transmitting signals representing binary 1 and binary 0

Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy

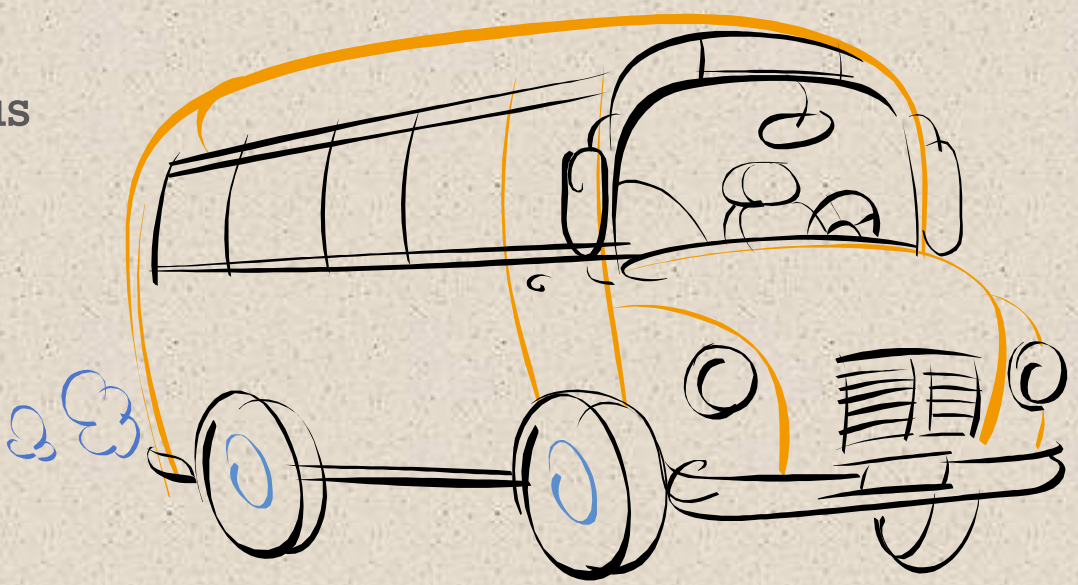
System bus

- A bus that connects major computer components (processor, memory, I/O)

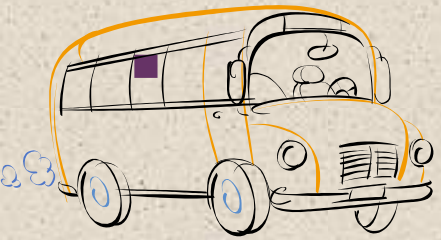
The most common computer interconnection structures are based on the use of one or more system buses

Data Bus

- Data lines that provide a path for moving data among system modules
- May consist of 32, 64, 128, or more separate lines
- The number of lines is referred to as the *width* of the data bus
- The number of lines determines how many bits can be transferred at a time
- The width of the data bus is a key factor in deciding overall system performance

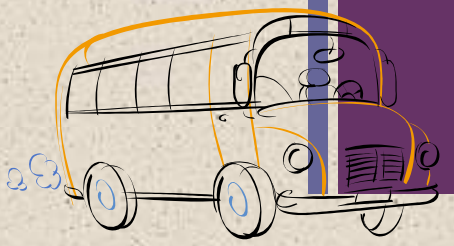


Address Bus



- Used to select the source or destination of the data on the data bus
  - If the processor wishes to read a word of data from memory it puts the address of the desired word on the address lines
- Width determines the maximum possible memory capacity of the system
- Also used to address I/O ports
  - The higher order bits are used to select a particular module on the bus and the lower order bits select a memory location or I/O port within the module

Control Bus



- Used to control the access and the use of the data and address lines
- Because the data and address lines are shared by all components there must be a means of controlling their use
- Control signals transmit both command and timing information among system modules
- Timing signals indicate the validity of data and address information
- Command signals specify operations to be performed

Bus Interconnection Scheme

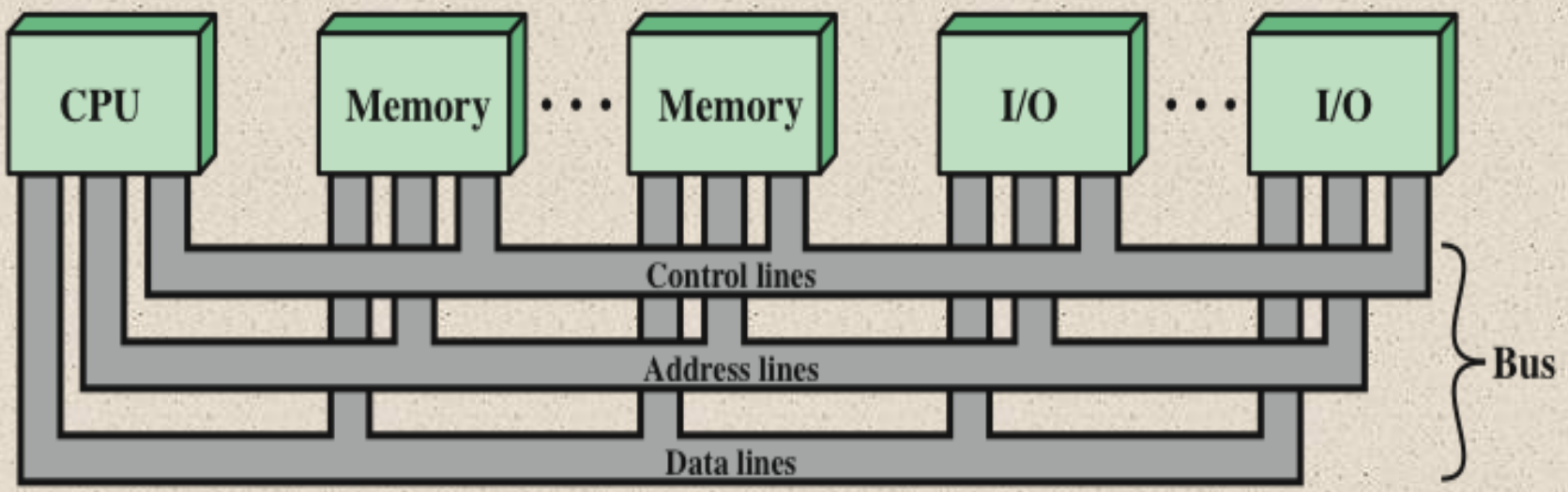
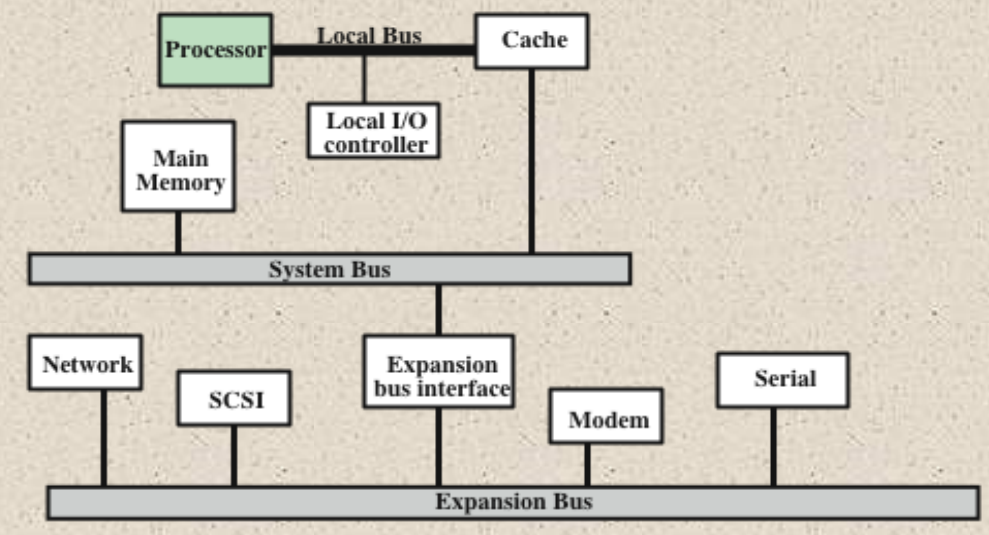
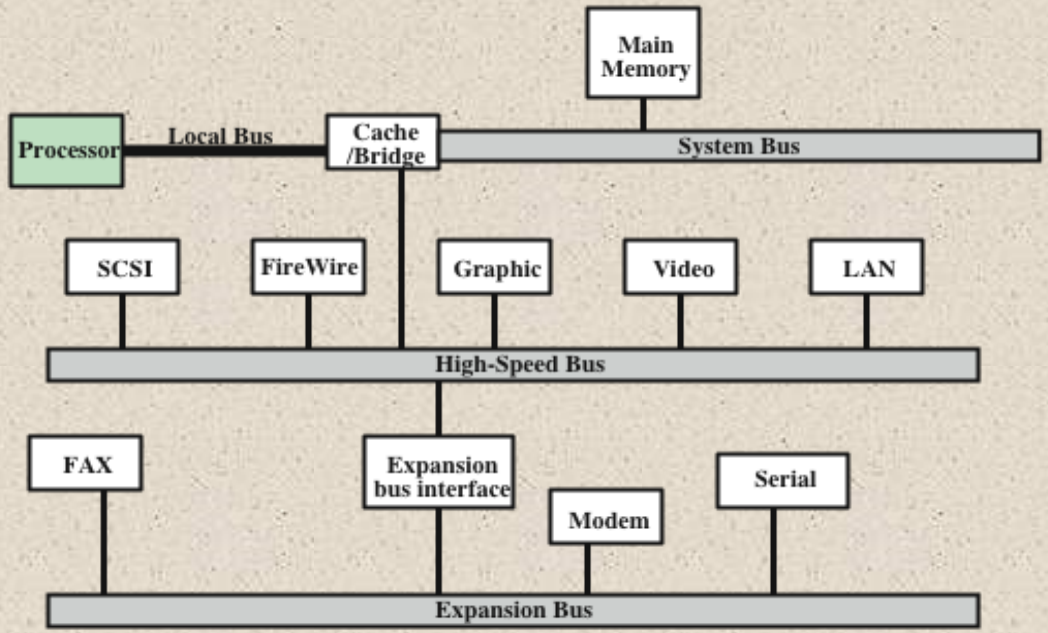


Figure 3.16 Bus Interconnection Scheme



(a) Traditional Bus Architecture



(b) High-Performance Architecture

Figure 3.17 Example Bus Configurations

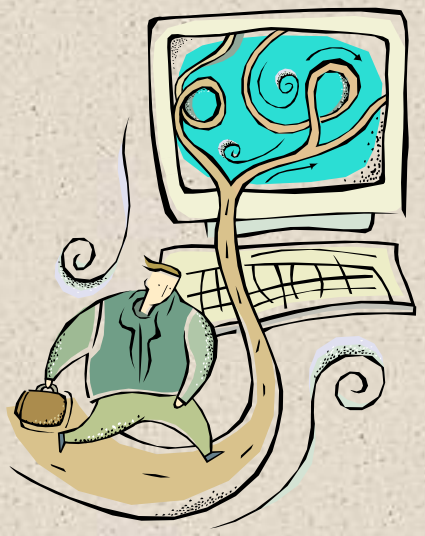
B- **Point-to-point Interconnect**

- The shared bus architecture was the standard approach to interconnection between the processor and other components (memory, I/O, and so on) for decades.
- But modern systems increasingly rely on point-to-point interconnection rather than shared buses.
- Compared to the shared bus, the point-to point interconnect has lower latency, higher data rate, and better scalability.
- we look at an important and representative example of the point-to-point interconnect approach: Intel's **Quick Path Interconnect (QPI)**, which was introduced in 2008.

Quick Path Interconnect

- Introduced in 2008
- Multiple direct connections
  - Direct pairwise connections to other components eliminating the need for arbitration found in shared transmission systems
- Layered protocol architecture
  - These processor level interconnects use a layered protocol architecture rather than the simple use of control signals found in shared bus arrangements
- Packetized data transfer
  - Data are sent as a sequence of packets each of which includes control headers and error control codes

QPI



Multicore Configuration Using QPI

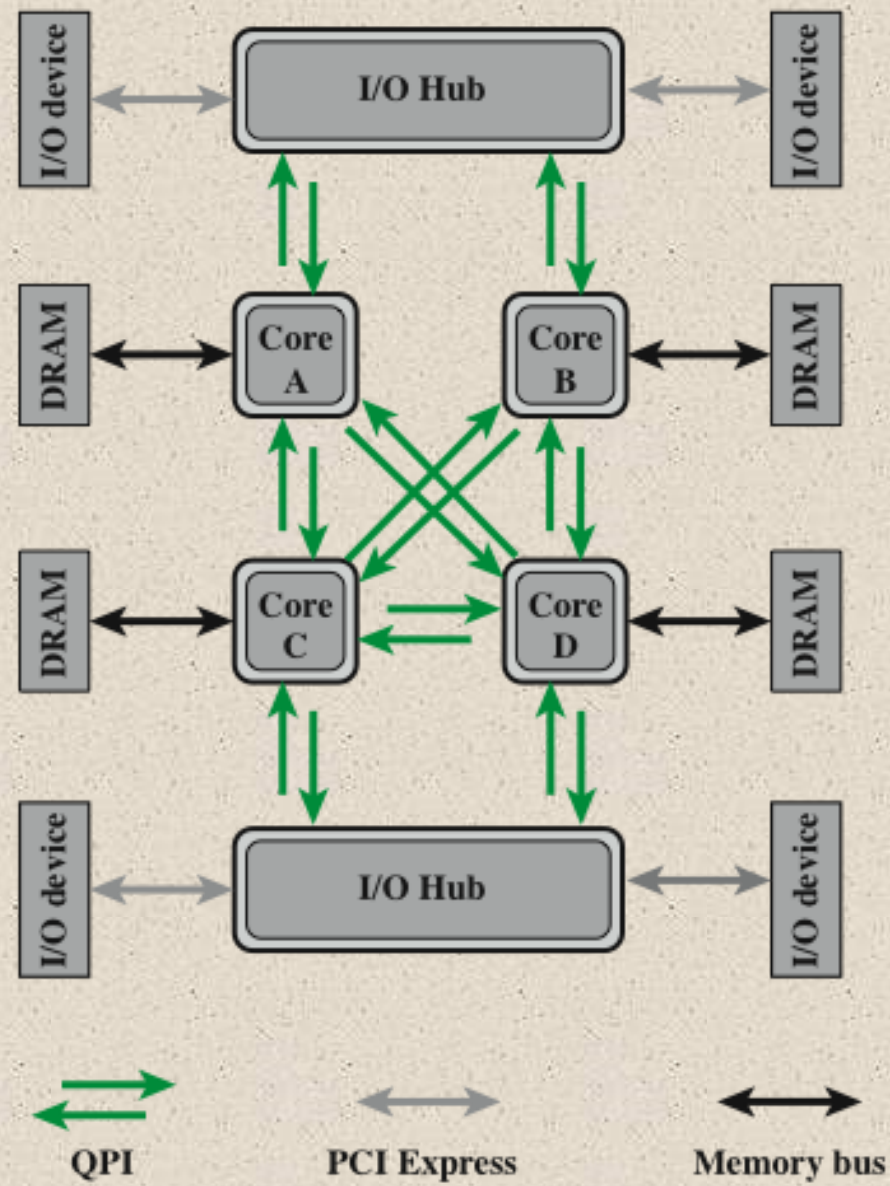


Figure 3.20 Multicore Configuration Using QPI

Figure 3.20 illustrates a typical use of QPI on a multi-core computer. The QPI links (indicated by the green arrow pairs in the figure) form a switching fabric that enables data to move throughout the network. Direct QPI connections can be established between each pair of core processors. If core A in Figure 3.20 needs to access the memory controller in core D, it sends its request through either cores B or C, which must in turn forward that request on to the memory controller in core D.

Similarly, larger systems with eight or more processors can be built using processors with three links and routing traffic through intermediate processors. In addition, QPI is used to connect to an I/O module, called an I/O hub (IOH).

The IOH acts as a switch directing traffic to and from I/O devices. Typically in newer systems, the link from the IOH to the I/O device controller uses an interconnect technology called PCI Express (PCIe), described later in this chapter. The IOH translates between the QPI protocols and formats and the PCIe protocols and formats. A core also links to a main memory module (typically the memory uses dynamic access random memory (DRAM) technology) using a dedicated memory bus.

QPI Layers

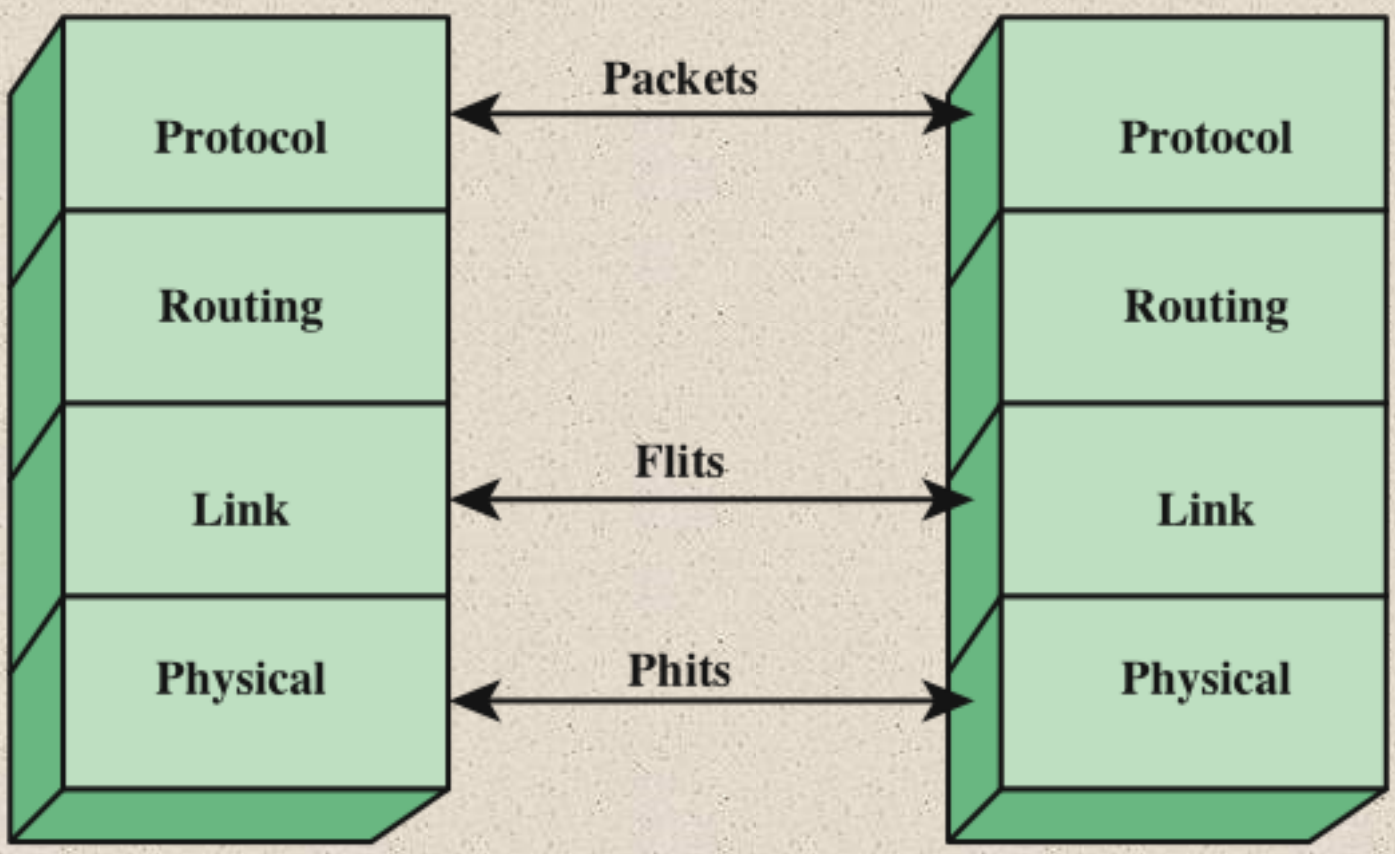


Figure 3.21 QPI Layers

QPI is defined as a four-layer protocol architecture, encompassing the following layers (Figure 3.21):

• **Physical:** Consists of the actual wires carrying the signals, as well as circuitry and logic to support helpful features required in the transmission and receipt of the 1s and 0s. The unit of transfer at the Physical layer is 20 bits, which is called a **Phit** (physical unit).

Link: Responsible for reliable transmission and flow control. The Link layer's unit of transfer is an 80-bit **Flit** (flow control unit).

• **Routing:** Provides the framework for directing packets through the fabric.

• **Protocol:** The high-level set of rules for exchanging **packets** of data between devices. A packet is comprised of an integral number of Flits.

Peripheral Component Interconnect (PCI)

- A popular high bandwidth, processor independent bus that can function as a mezzanine or peripheral bus
- Delivers better system performance for high speed I/O subsystems
- PCI Special Interest Group (SIG)
  - Created to develop further and maintain the compatibility of the PCI specifications
- PCI Express (PCIe)
  - Point-to-point interconnect scheme intended to replace bus-based schemes such as PCI
  - Key requirement is high capacity to support the needs of higher data rate I/O devices, such as Gigabit Ethernet
  - Another requirement deals with the need to support time dependent data streams

PCIe Configuration

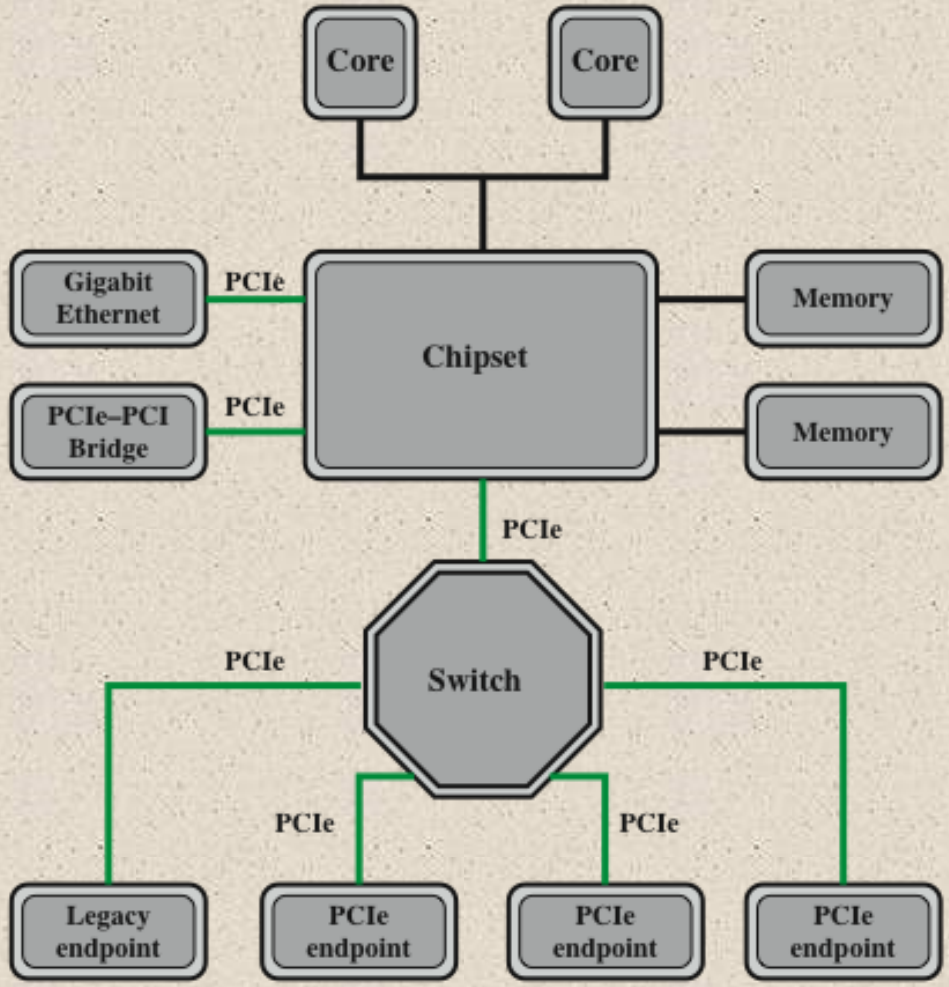


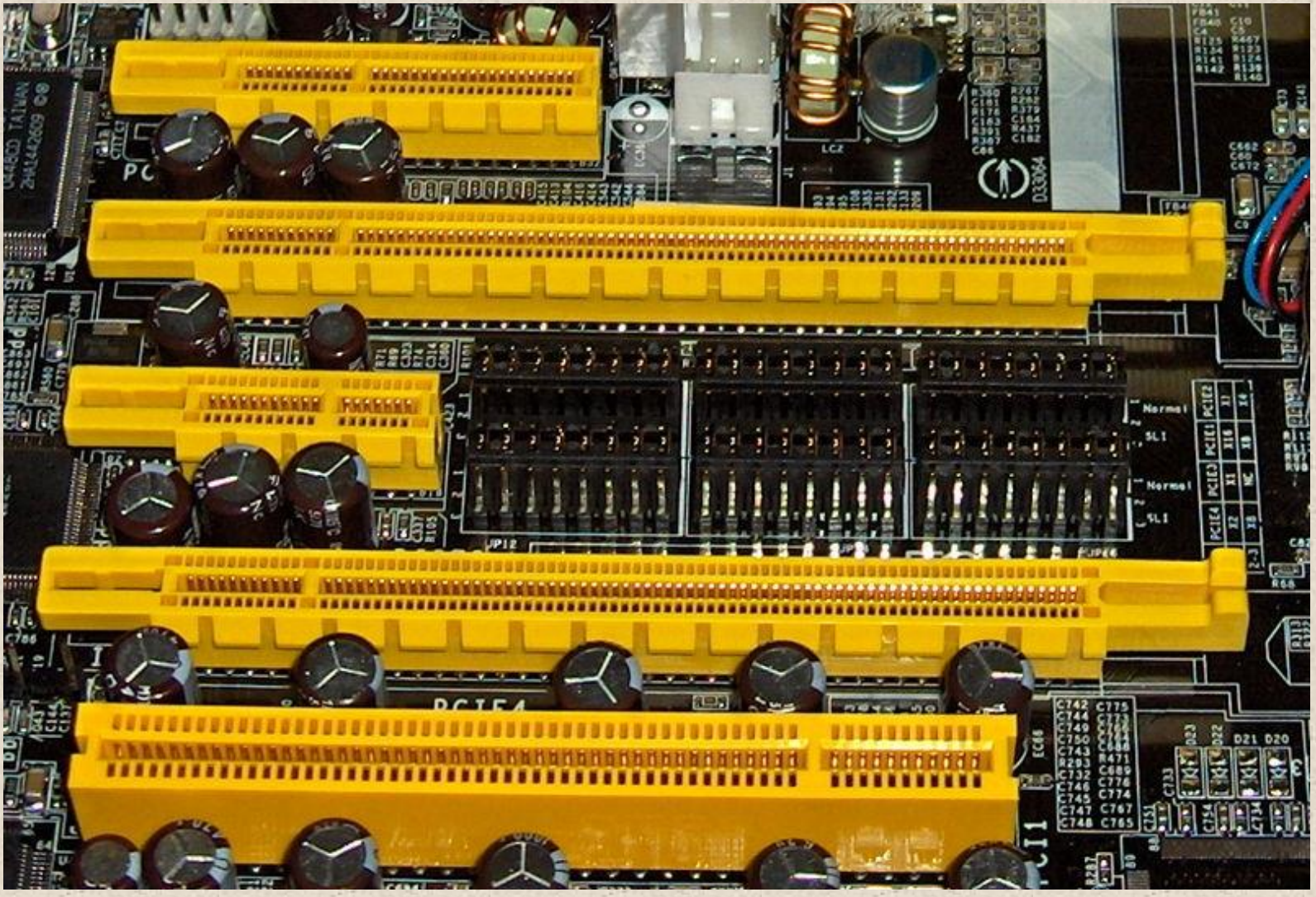
Figure 3.24 Typical Configuration Using PCIe

- Figure 3.24 shows a typical configuration that supports the use of PCIe.
- A root complex device, also referred to as a chipset or a host bridge, connects the processor and memory subsystem to the PCI Express switch fabric consisting one or more PCIe and PCIe switch devices.
- The root complex acts as a buffering device, to deal with difference in data rates between I/O controllers and memory and processor components.
- The root complex also translates between PCIe transaction formats and the processor and memory signal and control requirements.
- The chipset will typically support multiple PCIe ports, some of which attach directly to a PCIe device and one or more that attach to a switch that manages multiple PCIe streams.

PCIe links from the chipset may attach to the following kinds of devices that implement PCIe:

- **Switch:** The switch manages multiple PCIe streams.
- **PCIe endpoint:** An I/O device or controller that implements PCIe, such as a Gigabit Ethernet switch, a graphics or video controller, disk interface, or a communications controller.
- **Legacy endpoint:** Legacy endpoint category is intended for existing designs that have been migrated to PCI Express, and it allows legacy behaviors such as use of I/O space and locked transactions. PCI Express endpoints are not permitted to require the use of I/O space at runtime and must not use locked transactions. By distinguishing these categories, it is possible for a system designer to restrict or eliminate legacy behaviors that have negative impacts on system performance and robustness.
- **PCIe/PCI bridge:** Allows older PCI devices to be connected to PCIe-based systems.

PCI Express bus card slots (from top to bottom: x4, x16, x1 and x16), compared to a traditional 32-bit PCI bus card slot (bottom). (PCI = Peripheral Component Interconnect)



PCIe Protocol Layers

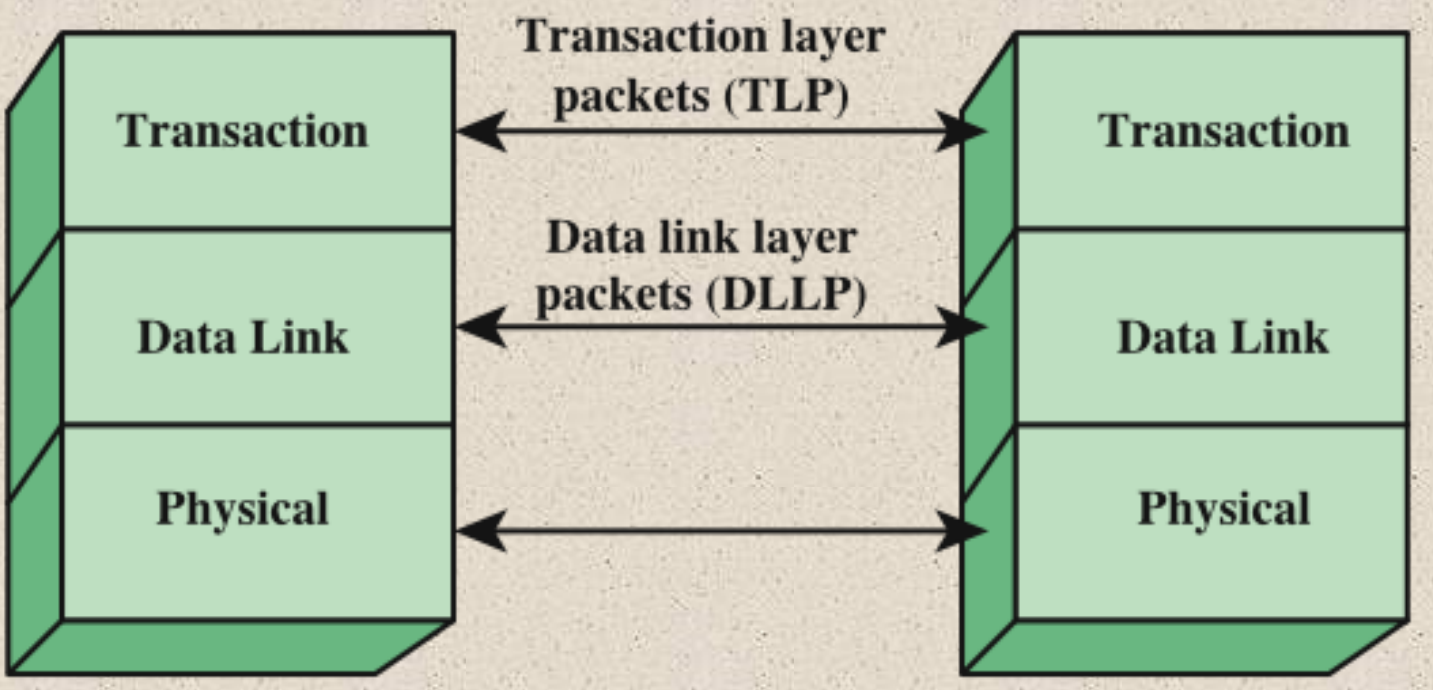


Figure 3.25 PCIe Protocol Layers

- As with QPI, PCIe interactions are defined using a protocol architecture. The PCIe protocol architecture encompasses the following layers (Figure 3.25):
  - **Physical:** Consists of the actual wires carrying the signals, as well as circuitry and logic to support helping features required in the transmission and receipt of the 1s and 0s.

  - **Data link:** Is responsible for dependable transmission and flow control. Data packets generated and consumed by the DLL are called Data Link Layer Packets (DLLPs).

  - **Transaction:** Generates and consumes data packets used to implement load/store data transfer mechanisms and also manages the flow control of those packets between the two components on a link. Data packets generated and consumed by the TL are called Transaction Layer Packets (TLPs).

- Above the TL are software layers that generate read and write requests that are transported by the transaction layer to the I/O devices using a packet-based transaction protocol.

Homework

Chapter 2

Performance Issues

All HW Hand on 08/10/2018

3.4 What types of transfers must a computer's interconnection structure (e.g., bus) support?

3.5 List and briefly define the QPI protocol layers.

3.6 List and briefly define the PCIe protocol layers.

Assignments : Hand on 08/10/2018

1. Write about registers ?
2. Make comparison between Traditional System Bus ,QPI ,PCI .